

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	456	703/22.ccor.	US-PGPUB; USPAT	OR	ON	2006/09/17 18:38
L2	390	703/13.ccor.	US-PGPUB; USPAT	OR	ON	2006/09/17 18:38
L3	126	703/17.ccor.	US-PGPUB; USPAT	OR	ON	2006/09/17 18:38
L4	128	703/19.ccor.	US-PGPUB; USPAT	OR	ON	2006/09/17 18:38
L5	364	virtual adj clock	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L6	48968	master and slave	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L7	19	L5 and L6	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L8	246	virtual adj real adj time	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L9	4	L5 and L8	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L10	7	L6 and L8	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L11	122	L5 and simulat\$\$	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L12	9	L6 and L11	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L13	6160	master near4 module	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L14	2679	slave near4 module	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L15	1833	L13 and L14	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L16	2	L5 and L15	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L17	996	L15 and command	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38

## EAST Search History

L18	618	L17 and clock	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L19	476	L18 and synchroni\$6	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L20	147	L19 and virtual	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L21	88	L20 and (real adj time)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L22	84	L21 and controller	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L23	18	L22 and socket	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L24	65	L22 and @ad<="20030806"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2006/09/17 18:38
L25	43	("5025364"   "5493508"   "5493672"   "5515525"   "5546562"   "5590049"   "5600579"   "5600790"   "5623418"   "5663900"   "5664098"   "5673418"   "5675771"   "5678028"   "5768567"   "5771370"   "5787245"   "5801958"   "5809450"   "5812431"   "5815715"   "5819065"   "5838948"   "5848236"   "5848270"   "5857091"   "5862361"   "5867399"   "5867400"   "5870308"   "5870585"   "5870588"   "5872958"   "5886899"   "5909578"   "5913052"   "5918035"   "5943490"   "5946472"   "5960181"   "5960182"   "5963724"   "6009256").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/09/17 18:38
L26	15	("6230114").URPN.	USPAT	OR	ON	2006/09/17 18:38

		Results
9.	((pub-date > 1959 and pub-date < 2004 and FULL-TEXT(test bed) and FULL-TEXT(flight)) and simulat!) and master) and slave [All Sources(- All Sciences -)]	14
8.	((pub-date > 1959 and pub-date < 2004 and FULL-TEXT(test bed) and FULL-TEXT(flight)) and simulat!) and master [All Sources(- All Sciences -)]	36
7.	(pub-date > 1959 and pub-date < 2004 and FULL-TEXT(test bed) and FULL-TEXT(flight)) and simulat! [All Sources(- All Sciences -)]	221
6.	pub-date > 1959 and pub-date < 2004 and FULL-TEXT(test bed) and FULL-TEXT(flight) [All Sources(- All Sciences -)]	356
5.	(((pub-date > 1959 and pub-date < 2004 and FULL-TEXT((master and slave)) and FULL-TEXT(synchronize)) and simulat!) and clock) and virtual [All Sources(- All Sciences -)]	19
4.	((pub-date > 1959 and pub-date < 2004 and FULL-TEXT((master and slave)) and FULL-TEXT(synchronize)) and simulat!) and clock [All Sources(- All Sciences -)]	71
3.	(pub-date > 1959 and pub-date < 2004 and FULL-TEXT((master and slave)) and FULL-TEXT(synchronize)) and simulat! [All Sources(- All Sciences -)]	155
2.	pub-date > 1959 and pub-date < 2004 and FULL-TEXT((master and slave)) and FULL-TEXT(synchronize) [All Sources(- All Sciences -)]	257
1.	pub-date > 1959 and pub-date < 2004 and FULL-TEXT(virtual real time) [All Sources(- All Sciences -)]	24

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		Results
<u>#1</u>	((virtual real time) <and> (pyr >= 1951 <and> pyr <= 2003)	21
<u>#2</u>	((master<and>slave<and>simulat*) <and> (pyr >= 1951 <and> pyr <= 2003)	3612
<u>#3</u>	((master<and>slave<and>simulat*)<and>synchroni*) <and> (pyr >= 1951 <and> pyr <= 2003)	1368
<u>#4</u>	((master<and>slave<and>simulat*)<and>synchroni*<and>(virtual clock)) <and> (pyr >= 1951 <and> pyr <= 2003)	9
<u>#5</u>	((master<and>slave<and>simulat*)<and>synchroni*<and>clock) <and> (pyr >= 1951 <and> pyr <= 2003)	812
<u>#6</u>	((master<and>slave<and>simulat*) <and>synchroni*<and>clock<and>virtual) <and> (pyr >= 1951 <and> pyr <= 2003)	216
<u>#7</u>	((master<and>slave<and>simulat*) <and>synchroni*<and>clock<and>virtual<and>socket) <and> (pyr >= 1951 <and> pyr <= 2003)	42
<u>#8</u>	((master<and>slave<and>simulat*) <and>synchroni*<and>clock<and>virtual<and>command) <and> (pyr >= 1951 <and> pyr <= 2003)	99
<u>#9</u>	((master<and>slave<and>simulat*) <and>synchroni*<and>clock<and>virtual<and>command<and>socket) <and> (pyr >= 1951 <and> pyr <= 2003)	26

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## Scholar

Results 1 - 7 of 7 for **master and slave and simulation and synchronize and "virtual clock" and socket**. (0.09 seconds)

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[S Lin](#)  
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**DIPART, An Interactive Simulation Platform For Studying Plan Development And Monitoring In Dynamic ... - group of 2 »**  
 TF Znatiith - ieeexplore.ieee.org  
 ... Transportation planning— a prototype simulation system that ... The concept of **virtual clock** has been widely used to support the **synchronization** of activities in ...  
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**[ps] 8.3 Media Call/Connection Scenarios - group of 2 »**

M Slave - cis.upenn.edu  
 ... ATM Card Network Bus (**master**) Operator Side Bus (**slave**) Robot Side ... force ring buer",\Write position into **socket**",\Read force from **socket**") reside in non- ...  
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S Lin, A Pan, Z Zhang, R Guo, Z Guo - Proc of HotOS - usenix.org  
 ... to maintain one code for **simulation** and another for real deployment, and try to sync up as ... The WiDS parallel **simulation** is **master-slave** architected and ...  
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R Tammana - 2003 - purl.fcla.edu  
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 ... Entwicklung: 1974: 1. SNA-NW: nur zentrales NW (Baumstruktur, 1 Host, n Terminals: typisches "DFV"-System - **Master/Slave-Prinzip**) 1976: mehrere Hosts ...  
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Searching for **virtual and clock and master and slave and simulation**.

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10 documents found. Order: **number of citations**.

[Typhoon-Zero Implementation: The Vortex Module - Pfile \(1995\) \(Correct\) \(13 citations\)](#)

protocols. These are: fine-grain access control, **virtual** memory management, efficient (low overhead)

: 30 7.1.1 **Clock** Speed :

<ftp.cs.wisc.edu/tech-reports/reports/95/tr1290.ps.Z>

One or more of the query terms is very common - only partial results have been returned. Try [Google \(CiteSeer\)](#).

[PAM-Blox: High Performance FPGA Design for Adaptive Computing - Mencer, Morf, Flynn \(1998\) \(Correct\) \(13 citations\)](#)

-with design tools -is investigated in the **Virtual Wires**[17] project. Eliminating the pin

Sram Sram Dram Cpu Main Memory Main Memory Bus **Clocks** Interface Pci Lca3 Lca1 Lca0 Lca2 Pif E E E on the host system. PCI Pamette can operate in **master** and **slave** mode on the PCI bus. A flexible user <arith.stanford.edu/oskar/fccm98.ps>

[Visualization of Parallel Execution Graphs - Steckelbach, Bubeck, Fößmeier.. \(Correct\)](#)

or times provide only information about the **virtual** process time. For multithreaded processes, this has to be accounted to each thread. Measuring wall **clock** time is completely inadequate, since the Host "linus" Fig. 1. Control flow for a single **master** and a single **slave** thread 3 A Graph Theoretical <www.ti.informatik.uni-tuebingen.de/~ritt/Publications/Gravis.ps>

[Finite Element Message-Passing/DSM Simulation Algorithm.. - Plazek, Banas, Kitowski \(Correct\)](#)

On HP/Convex SPP 1600 system processes run on **virtual** machines called subcomplexes, which are P, DSM, 6 iter. P4x4, DSM, 6 iter. Fig. 1. Wall-clock execution time for one **simulation** step for two different processing units. There exists one **master** process that controls the solution procedure and <www.icsr.agh.edu.pl/publications/ps/hp98-post.ps.gz>

[Requirements for the Simulation of Distributed Protocols - Spirakis, Tampakas.. \(1996\) \(Correct\)](#)

62 1. The **Virtual** Path Layout Algorithm of Gerstel -

7 1. The **Clock** Synchronization Algorithm of L.

<helios.cti.gr/alcom-it/dsp/dspreq.ps.gz>

[Parallel Discrete-Event Simulation Using Pvm - Wentong Cai \(1994\) \(Correct\)](#)

a scheduling algorithm is required. PVM (Parallel **Virtual** Machine) is a software package that allows the nullmessages are used to advance the **simulation clock** and thus to avoid deadlocks. The optimistic models: SPMD (Single Program Multiple Data) or **master/slave**. We adopted the **master/slave** model in our [sentosa.sas.ntu.ac.sg:8000/~zhum/ps\\_files/hpcc94.ps.Z](sentosa.sas.ntu.ac.sg:8000/~zhum/ps_files/hpcc94.ps.Z)

[Aiaa-98-4707 - American Institute \(Correct\)](#)

Often, it is desired to use these **simulations** as **virtual** prototypes to obtain an acceptable or optimized

Figure 2 shows the optimization wall **clock** histories for serial and parallel CPS. With 3 are discussed, although emphasis is given to a **master/slave** implementation using the Message Passing [endo.sandia.gov/9234/.sd\\_optim/MDO98\\_paper.ps.gz](endo.sandia.gov/9234/.sd_optim/MDO98_paper.ps.gz)

[Functional Verification of the RCMP Egress Routing Logic - Palanisamy, Tahar \(1998\) \(Correct\)](#)

and (4) OAM cell processing and routing for 64K **virtual** channels. The RCMP supports Ingress function made on the Egress logic are [4]1) The same **clock** is used for the PHY interface and the Switch

Figure 1. RCMP Switch Fabric Egress MultiMaster -**master** logic logic Multi PHY #32 PHY #2 #1

[www.ece.concordia.ca/~tahar/pub/Egress\\_TR98.ps](www.ece.concordia.ca/~tahar/pub/Egress_TR98.ps)

[PANNS - A Parallelized Artificial Neural Network Simulator - Thomas Furle \(Correct\)](#)

were met, multithreading, remote links, **virtual** units, and processor synchronisation. 2.1.1

t .physical timestamp i Figure 5: Logical **clock** To avoid the creation of pseudo links, which are

Distribution of Neurons on a Cluster Process 0 (**Master**) Neuron 0 Neuron 1 Neuron 1 Neuron 0 Neuron

<www.pri.univie.ac.at/~schiki/research/paper/iconip97/iconip97.ps>

- **Flexible codesign target architecture for early...** - Tammemäe, O'Nils, Hemani (Correct)

We are using a Xilinx XC4013 FPGA based Engineer's Virtual Computer board [4] connected to the SBus of is simulated from HW side, thus establishing real **clock-level simulation**. Coemulation. Hardware is taken from [11] expressing unambiguously **master-slave** relationship between SW and HW. 2 AKKA's [www.ele.kth.se/ESD/doc/ar96/nalle/springer.ps.gz](http://www.ele.kth.se/ESD/doc/ar96/nalle/springer.ps.gz)

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